

Atty. Docket No. OPP-GZ-2007-0009-US-00  
Application No: 10/676,645

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Amendments to the Claims

Please amend the Claims as shown below. This listing of Claims replaces all prior versions and listings of the Claims in this application.

Listing of Claims

1. (Currently Amended) A bonding pad of a semiconductor device comprising:  
a via within an insulation layer over a semiconductor substrate metal line;  
a barrier metal layer on a surface of the via;  
a metal line consisting essentially of copper layer in the via over on the barrier metal layer within the via, the copper layer having vertical side surfaces that contact the barrier metal layer;  
a pad in a predetermined region of the metal line; and  
an alloy layer on an upper surface of the metal line copper layer within the via, the alloy having a top surface that is coplanar with or lower than a top surface of the insulation layer, whrcin and vertical side surfaces that of the alloy layer contact the barrier metal layer within the via, wherein and the alloy layer consists essentially of copper and a low melting point metal selected from the group consisting of aluminum, lead, and silver.
2. (Canceled)
3. (Canceled)
4. (Currently Amended) The bonding pad semiconductor device of claim 1, whrcin a thickness of the alloy layer is less than a thickness of the metal line copper layer.
5. (Currently Amended) The bonding pad semiconductor device of claim 1, further comprising a protection layer comprising silicon nitride or silicon oxynitride on over the metal line copper layer except for the portion of the copper layer within the via predetermined region.

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6. (Canceled)

7. (Canceled)

8. (Currently Amended) The bonding pad semiconductor device of claim 5, wherein a width of the bonding pad is less than a width of the via.

9-20. (Canceled)

21. (Canceled)

22. (Currently Amended) The bonding pad semiconductor device of claim 1, wherein a width of the bonding pad is less than a width of the via.

23. (Currently Amended) The bonding pad semiconductor device of claim 1, wherein the barrier metal comprises a metal selected from a group consisting of Ti, Ta, TiN, and TaN.

24. (Currently Amended) The bonding pad semiconductor device of claim 1, wherein the barrier metal has a thickness between 200 and 800 Å.

25. (Cancelled)

26. (Cancelled)

27. (Currently Amended) The bonding pad semiconductor device of claim 1, wherein the insulation layer comprises an oxide layer.

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28. (Currently Amended) The bonding pad semiconductor device of claim 23, wherein the barrier metal layer prevents the diffusion of copper from the metal line-copper layer into the insulating layer substrate.

29. (Currently Amended) The bonding pad semiconductor device of claim 1, wherein the alloy layer is completely within the via.

30. (Currently Amended) The bonding pad semiconductor device of claim 1, wherein the barrier metal layer covers all surfaces of the via.

31. (Currently Amended) The bonding pad semiconductor device of claim 5, wherein the alloy layer is exposed through an opening in the protection layer.

32. (Currently Amended) The bonding pad semiconductor device of claim 1, wherein the barrier metal layer has a thickness of ~500 Å.

33. (Canceled)

34. (Currently Amended) The bonding pad semiconductor device of claim 1, wherein the barrier metal layer contacts the insulating layer substrate.

35. (Currently Amended) The bonding pad semiconductor device of claim 5, wherein the bonding pad is exposed through an opening in the protection layer.

36. (Currently Amended) The bonding pad semiconductor device of claim 1, wherein the alloy layer comprises copper and aluminum.

37. (Currently Amended) The bonding pad semiconductor device of claim 1, wherein the alloy layer comprises copper and either lead or silver.